Electronic Version
Stylesheet Version v1.1.1

Claims

[c1] A method of making a buried plate region in a semiconductor substrate, comprising:
forming a trench in a semiconductor substrate, the trench having a trench sidewall, the sidewall including an upper portion, and a lower portion disposed below the upper portion;
forming a liner along at least the lower portion of the trench sidewall;
thereafter forming a dopant source layer over the liner, the dopant source layer not being disposed along the upper portion of the trench sidewall; and
annealing the semiconductor substrate to drive a dopant from the dopant source layer into the semiconductor substrate adjacent to the lower portion of the trench sidewall while preventing the dopant from being driven into the semiconductor substrate adjacent to the upper portion of the trench sidewall.

[c2] A method as claimed in claim 1, wherein a cap layer is formed in the trench to prevent the dopant from being driven into the semiconductor substrate adjacent to the upper portion.

[c3] A method as claimed in claim 1, wherein the liner is formed by thermal nitridation.

[c4] A method as claimed in claim 3, wherein the liner has a thickness of between about 7 Å and 10 Å.

[c5] A method as claimed in claim 1, wherein the liner is formed by thermal oxidation.

[c6] A method as claimed in claim 3, wherein the liner has a thickness of about 20 Å.

[c7] A method as claimed in claim 1, wherein the cap layer consists essentially of an oxide.

[c8] A method as claimed in claim 1, wherein the cap layer consists essentially of an undoped oxide.

[c9] A method as claimed in claim 1, wherein the cap layer is a nitride layer.

[c10] A method as claimed in claim 1, wherein the annealing is conducted at a temperature of above about 900 °C.

[c11] A method as claimed in claim 1, wherein the annealing is conducted at a temperature of about 1050 °C.

[c12] A method as claimed in claim 1, further comprising removing the cap layer, the dopant source layer and the

liner from the trench sidewall after the annealing, and thereafter etching material of the substrate exposed at the trench sidewall selectively to lightly doped semiconductor material, whereby the more heavily doped semiconductor material present at the lower portion of the trench sidewall is etched more rapidly than the more lightly doped semiconductor material present at the upper portion to widen the trench along the lower portion.

[c13] A method as claimed in claim 1, further comprising removing the cap layer, the dopant source layer and the liner from the trench sidewall after the annealing, thereafter forming a collar along the upper portion of the trench sidewall, and then widening the lower portion of the trench sidewall.

[c14] A method as claimed in claim 1, wherein the dopant source layer is formed by depositing arsenic doped glass (ASG) at a temperature of about 700 °C.

[c15] A method of making a trench capacitor having a buried plate formed according to a method as claimed in claim 1, further comprising:
forming a node dielectric along the lower portion of the trench sidewall after removing the liner and the dopant source layer; and
depositing at least one of a conductive and a semicon-

ducting material onto the node dielectric as a second plate opposing the buried plate.

[c16] The method of claim 1 wherein the liner and the dopant source layer are formed in the lower portion of the trench sidewall by forming the liner, forming the dopant source layer over the liner, depositing a cover material over the dopant source layer, recessing the cover material to a predetermined level, and removing the liner and the dopant source layer from the upper portion of the trench sidewall.

[c17] A method of forming a trench in a semiconductor substrate and a buried plate in the semiconductor substrate adjacent to a lower portion of the trench sidewall, comprising:
forming a pad stack on a semiconductor substrate and patterning the pad stack to form an opening;
patterning a trench through the opening by vertically etching the substrate selective to a material of the pad stack;
forming a liner on the semiconductor substrate along a sidewall of the trench;
forming a dopant source layer over the liner on a lower portion of the trench sidewall;
forming a cap layer covering at least an upper portion of the trench sidewall above the lower portion; and

annealing to drive a dopant from the dopant source layer into the single-crystal semiconductor material of the substrate adjacent to the lower portion to form a buried plate.

[c18] A method as claimed in claim 17, wherein the dopant source layer includes arsenic doped glass, the liner is formed by at least one of thermal oxidation and thermal nitridation, and the cap layer consists essentially of an undoped oxide.

[c19] A method of forming a trench capacitor in a semiconductor substrate, comprising:
forming a pad stack on a semiconductor substrate and patterning the pad stack to form an opening;
patterning a trench through the opening by vertically etching the substrate selective to a material of the pad stack;
forming a liner on the semiconductor substrate along a sidewall of the trench;
forming a dopant source layer over the liner;
removing the dopant source layer from the liner along an upper portion of the trench sidewall, while allowing the dopant source layer to remain along a lower portion of the trench sidewall disposed below the upper portion;
forming a cap layer covering at least the upper portion of the trench sidewall;

annealing to drive a dopant from the dopant source layer into the semiconductor material of the substrate adjacent to the lower portion to form a buried plate;
removing the cap layer, the dopant source layer and the liner from at least the lower portion of the trench sidewall;
forming a node dielectric along the lower portion of the trench sidewall; and
forming a node electrode on a side of the node dielectric opposite the buried plate.

[c20] A method as claimed in claim 19, wherein the liner is formed by at least one of thermal oxidation and thermal nitridation, the dopant source layer includes arsenic doped glass (ASG), and the cap layer consists essentially of an undoped oxide, the method further comprising widening the lower portion prior to forming the node dielectric and prior to forming the node electrode.